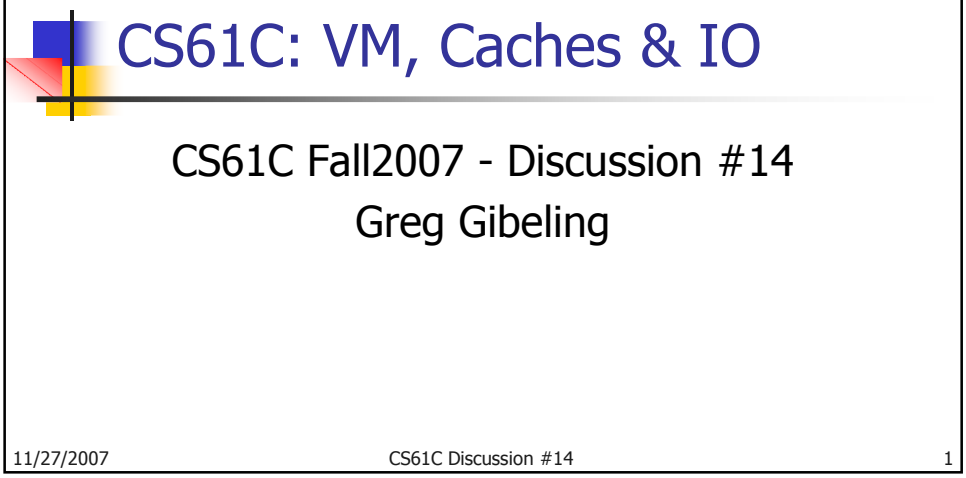


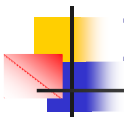
CS61C: VM, Caches & IO

CS61C Fall2007 - Discussion #14

Greg Gibeling

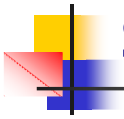
Possibilities

- Lecturing
  - VM & Cache Review
  - VM: Segmentation (x86/IA32)
  - IO Questions?
- Problems
  - Design an Inverted Page Table
  - Design a Serial Port for Proj4



Inverted Page Table

- Problem
  - You want to store one entry per-frame
    - Page: a block of virtual memory
    - Frame: a block of physical memory
  - Still need to be able to do V2P translation
  - Needs to be "fast"
- Results
  - Address translation flow chart
  - Data structure/memory layout
  - Format of a page table entry
  - Rough sketch of hardware involved



Serial Port for Proj4

- Problem
  - Interface a serial port to your proj4
  - Use Memory Mapped I/O (MMIO)
  - Serial Port Module

```
module SerialPort(Clock, Reset, TX, RX,
  InData, InRead, InReady, OutData,
  OutWrite);
```

- Results
  - Schematic (modifications to Fig5.24)
  - Memory/Register Map
  - Send "Hello, World!" over the serial port